MULTIMEDIA UNIVERSITY

STUDENT ID NO

MULTIMEDIA UNIVERSITY

FINAL EXAMINATION

TRIMESTER 2, 2018/2019

ECP4256 –PRACTICAL FPGA DESIGN AND INTERFACING

(TE / RE)

12 MARCH 2019
9.00 a.m. - 11.00 a.m.
(2 Hours)

INSTRUCTIONS TO STUDENTS

1. This question paper consists of 5 pages excluding the cover page with 5 Questions only.

2. Attempt ALL the questions. All questions carry equal marks and the distribution of the marks for each question is given.

3. Please write all your answers in the Answer Booklet provided.

Question 1

a) A code converter is designed to convert a 4 bit binary number to the corresponding Gray code number. The inputs of the binary number $x1\ x2\ x3\ x4$ are available in high and low assertion, where $x4$ is the low-order bit. The outputs for the Gray code $z1z2z3z4$ are asserted high, where z4 is the low-order bit. This binary to gray code conversion can be done by applying following rules:

1. The Most Significant Bit (MSB) of the gray code is always equal to the MSB of the given binary code.
2. Other bits of the output gray code can be obtained by XORing binary code bit at that index and previous index.

i. Complete the binary-to-Gray code conversion table as given in Table-1(a) [7 Marks]

ii. Obtain the simplified Boolean equations for $z1, z2, z3, and\ z4$ using Karnaugh map. [4 Marks]

iii. Implement the simplified Boolean equations of $z1, z2, z3, z4$ obtained in (ii) using Programmable Logic Array (PLA). [4 Marks]

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Table-1(a) Binary to Gray code Conversion

Binary				Gray			
$x1$	$x2$	$x3$	$x4$	$z1$	$z2$	$z3$	$z4$
0	0	0	0				
0	0	0	1				
0	0	1	0				
0	0	1	1				
0	1	0	0				
0	1	0	1				
0	1	1	0				
0	1	1	1				
1	0	0	0				
1	0	0	1				
1	0	1	0				
1	0	1	1				
1	1	0	0				
1	1	0	1				
1	1	1	0				
1	1	1	1				

b) The Altera Cyclone II FPGA M4K Memory block is shown in Figure-1(b). Explain any **FIVE (5)** memory modes supported by M4K Memory block.

[5 Marks]

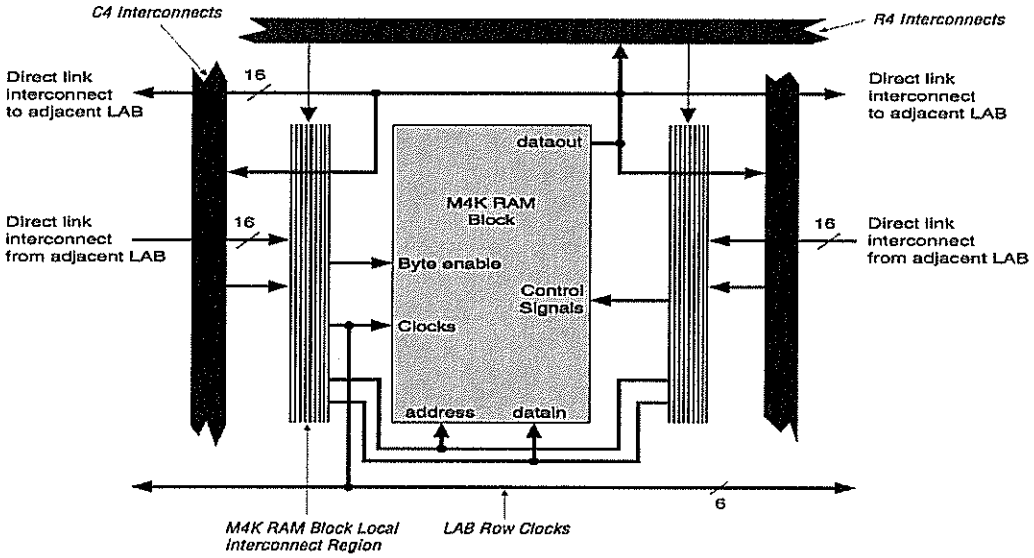

Figure-1(b) M4K Memory block

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Question 2

a) A LED seven segment display is shown in Figure-2(a).

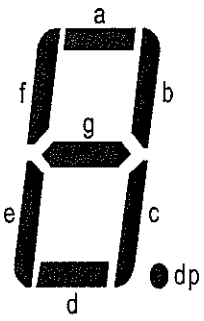

Figure-2(a) LED Seven Segment Display

i. Write the Verilog code for BCD to seven segment decoder. [15 Marks]

ii. Write the testbench to verify the functionality of seven segment decoder design in (i). [5 Marks]

Continued ...

Question 3

a) Explain briefly the concepts with Algorithmic State Machine(ASM) chart
   i. Loop unrolling [3 Marks]
   ii. Multi-cycling [3 Marks]

b) The ASM chart of 8X8 Sequential Matrix multiplication is shown in Figure-3(b).
   i. Explain how the performance can be improved by using loop unrolling by 2. [7 marks]

   ii. Explain how the performance obtained in (i) can be further improved using multi-cycling technique. [7 Marks]

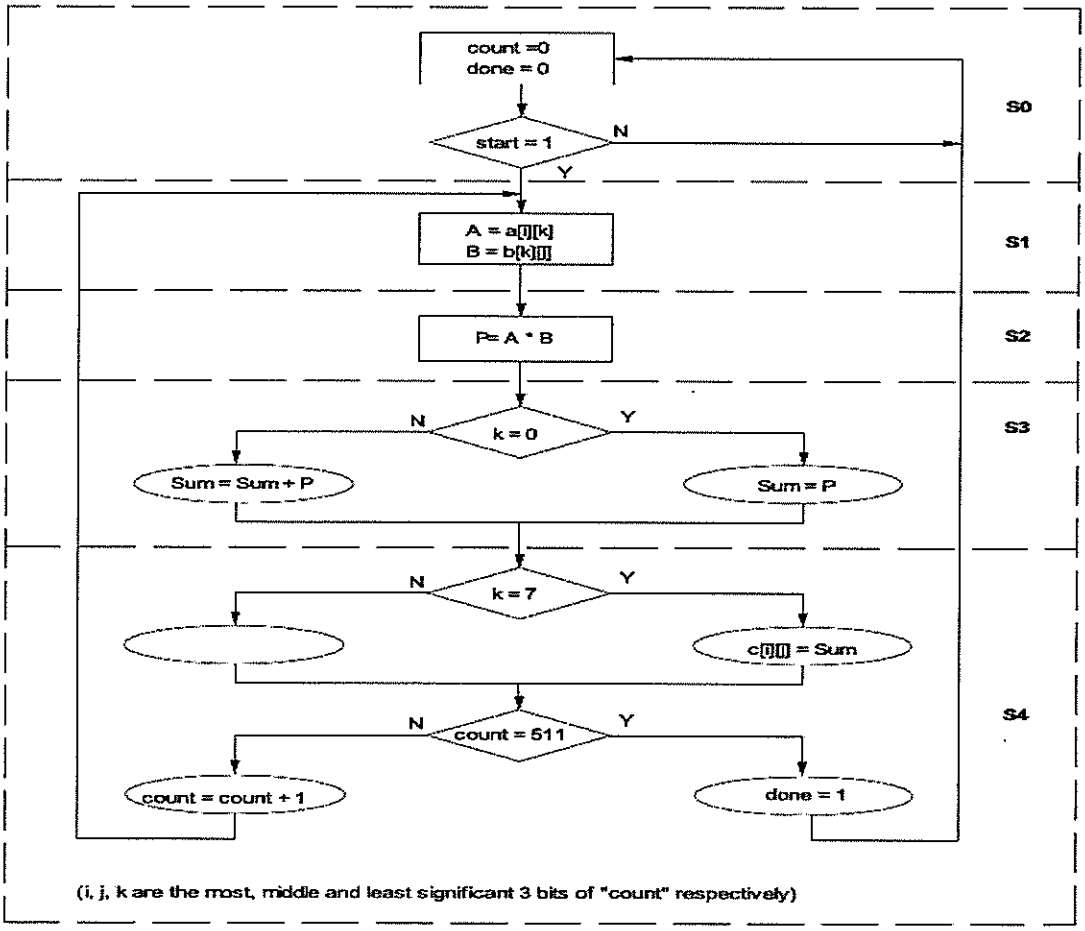

Figure-3(b) 8X8 Sequential Matrix multiplication

Continued ...

Question 4

a) Design a Finite state machine (FSM) of the sequence detector that outputs 1 when three consecutive ones (1's) have been received as input and zero (0) otherwise.

i. Draw the FSM for a Moore 111 sequence detector [5 marks]

ii. Write the Verilog code for a Moore 111 sequence detector. [12 marks]

iii. Redraw the FSM for a Mealy 111 sequence detector [3 marks]

Question 5

a) What is System on Chip (SoC)? What are the blocks included in typical SoC? [5 Marks]

b) Explain the important features of Hard and Soft processors of System on Programmable Chip (SoPC)? [5 Marks]

c) Design a SOPC system on Altera Cyclone II FPGA chip for a DVD Player with the following features.

- Disc reader (2 pairs LVDS, 1 x SPI)
  i. Video (LVDS)
  ii. Audio (LVDS)
  iii. Motor controller (SPI)
- Send video signal through HDMI to TV
- Send audio signal to speaker
  i. Digital audio codec with Bluetooth interface
- Front panel control
  i. 7 buttons (Parallel input)
  ii. Displays (I^2C)

Note: Use a block diagram to illustrate your design and describe the functionality of each block. [10 Marks]

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